

CLAIMS:

1. A semiconductor device comprising:
 - a semiconductor substrate having a cell array region and a peripheral circuit region;
 - a plurality of word line patterns placed on the cell array region;
 - 5 at least one gate pattern placed on the peripheral circuit region;
 - an interlayer insulating layer covering an upper surface of the semiconductor substrate having the word line patterns and the at least one gate pattern;
 - a self-aligned contact hole formed in the interlayer insulating layer between the word line patterns;
- 10 a self-aligned contact spacer covering a side wall of the self-aligned contact hole; and gate spacers interposed between side walls of the at least one gate pattern and the interlayer insulating layer, a width of the gate spacers being substantially different from a width of the self-aligned contact spacer.
- 15 2. The semiconductor device according to claim 1, further comprising:
 - word line spacers interposed between side walls of the word line patterns placed opposite to the self-aligned contact hole and the interlayer insulating layer, the word line spacers being formed of the same material layer as the gate spacer, the word line spacers having the same width as that of the gate spacers.
- 20 3. The semiconductor device according to claim 2, further comprising:
 - a spacer etch stop layer interposed between the word line spacers and the word line patterns, between the gate spacers and the at least one gate pattern, and between the self-aligned contact spacer and the word line patterns.
- 25 4. The semiconductor device according to claim 2, further comprising:
 - a contact etch stop layer interposed between the word line spacers and the interlayer insulating layer, and between the gate spacers and the interlayer insulating layer.
- 30 5. The semiconductor device according to claim 1, wherein the interlayer insulating layer is one selected from an HDP oxide layer, a USG layer, a BPSG layer, and a PSG layer.

6. The semiconductor device according to claim 1, wherein the self-aligned contact hole includes a lower contact hole formed at a region between the word line patterns, and an upper contact hole placed on the lower contact hole and formed to penetrate the interlayer insulating layer.

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7. The semiconductor device according to claim 6, wherein the diameter of the lower contact hole is less than that of the upper contact hole in a direction across the word line patterns.

10 8. The semiconductor device according to claim 1, wherein the width of the self-aligned contact spacer is smaller than the width of the gate spacers.

9. A device comprising:

at least two word line patterns in a cell array region of a semiconductor substrate;

15 at least one gate pattern in a peripheral circuit region of the semiconductor substrate;

an inter-layer insulating layer covering the semiconductor substrate, the at least two word line patterns, and the at least one gate pattern, the at least one gate pattern including a gate spacer interposed between a sidewall of the at least one gate pattern and the inter-layer insulating layer;

20 a self-aligned contact hole penetrating the inter-layer insulating layer between the at least two word line patterns; and

a self-aligned contact spacer on a sidewall of the self-aligned contact hole, a width of the self-aligned contact spacer unequal to a width of the gate spacer.

25 10. The device of claim 9, further comprising:

a word line spacer between one of the at least two word line patterns and the interlayer insulating layer, the word line spacer formed of the same material and having the same width as the gate spacer.

30 11. The device of claim 10, further comprising:

a spacer etch stop layer between the word line spacer and one of the at least two word line patterns, between the gate spacer and the at least one gate pattern, and between the self-aligned contact spacer and the at least two word line patterns.

12. The semiconductor device according to claim 10, further comprising:
a contact etch stop layer between the at least two word line spacers and the inter-layer insulating layer, and between the gate spacer and the inter-layer insulating layer.

5 13. The semiconductor device according to claim 9, the self-aligned contact hole comprising:

a lower contact hole; and

an upper contact hole, a diameter of the upper contact hole greater than a diameter of the lower contact hole in a direction perpendicular to the at least two word line patterns.

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14. A method of fabricating a semiconductor device comprising:
forming a plurality of word line patterns on a semiconductor substrate in a cell array region;

15 forming at least one gate pattern on the semiconductor substrate in a peripheral circuit region;

forming word line spacers on the side walls of the word line patterns and gate spacers on the side walls of the at least one gate pattern;

forming an interlayer insulating layer on an upper surface of the semiconductor substrate having the word line spacers and the gate spacers;

20 etching the interlayer insulating layer and the word line spacers to form a self-aligned contact hole penetrating a predetermined region between the word line patterns; and

forming a self-aligned contact spacer having a width different from that of the gate spacers on a side wall of the self-aligned contact hole.

25 15. The method according to claim 14, further comprising:

forming a spacer etch stop layer on the upper surface of the semiconductor substrate having the word line patterns and the at least one gate pattern before forming the word line spacers and the gate spacers, the spacer etch stop layer functioning as a buffer layer against the etching while the self-aligned contact hole or the self-aligned contact spacer is formed.

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16. The method according to claim 14, further comprising:
before forming the interlayer insulating layer, forming a contact etch stop layer on the upper surface of the semiconductor substrate having the word line spacers and the gate

spacers, the contact etch stop layer functioning as a buffer layer against the etching while the self-aligned contact hole is formed.

17. The method according to claim 14, wherein the word line spacers are formed
5 of the same insulating layer as the gate spacers.

18. The method according to claim 15, wherein the spacer etch stop layer is formed of an insulating layer having an etching selectivity ratio to the word line spacers and the gate spacers.

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19. The method according to claim 16, wherein the contact etch stop layer is formed of an insulating layer having an etching selectivity ratio to the interlayer insulating layer.

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20. The method according to claim 14, wherein the self-aligned contact spacer is formed of an insulating layer having an etching selectivity ratio to the interlayer insulating layer.